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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Yoshiyuki Yanagisawa et al.	**Atty. Docket No.**	075834.00085
Serial No.:	09/876,290	**Group Art Unit:**	2827
Filed:	June 7, 2001	**Examiner:**	David E. Graybill

Invention: "ASSEMBLY JIG AND MANUFACTURING METHOD OF MULTILAYER SEMICONDUCTOR DEVICE"

AMENDMENT A

Assistant Commissioner of Patents
Washington, D.C. 20231

S I R:

In response to the Office Action dated February 27, 2002, please amend the application as follows:

PETITION FOR EXTENSION OF TIME

Applicant hereby petitions for a two-month extension of time to respond to the outstanding Office Action under 37 C.F.R. §1.136(a). The time to respond is thus extended to July 27, 2002. Applicant has also included a check in the amount of $400.00 as payment of the required fee set forth in 37 C.F.R. §1.17(a).

IN THE CLAIMS:

1. A multilayer semiconductor device assembly jig, comprising:

[a base member for serially layering a plurality of semiconductor modules each including a semiconductor chip mounted on a thin printed-wiring board and a bump on each of a plurality of inter-layer connection lands;]

a lateral position restriction mechanism for [layering said] positioning a plurality of stacked semiconductor modules on [said] a base member with their respective lateral positions mutually restricted;

a height restriction mechanism for restricting an entire height of said semiconductor [module group]modules layered on said base member;

[an evenness holding mechanism for maintaining evenness of a top-layer

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semiconductor module;]and

an alignment mechanism for providing alignment with reference to a mother substrate [where a layered semiconductor module unit is mounted],

[wherein said assembly jig performs interlayer connection among said semiconductor modules by applying reflow heating to melt each of said bumps, is inverted to be positioned and combined with said mother substrate via said alignment mechanism, and is removed after the interlayer connection between this mother substrate and a first-layer semiconductor module of said layered semiconductor module unit].

2. The multilayer semiconductor device assembly jig according to claim 1 [having] comprising a box-shaped member which is [assembled] positioned on said base member and [comprises] having a storage space for storing [the specified number of] said semiconductor modules in a layered state,

wherein an inner wall of said storage space constitutes said lateral position restriction mechanism [by supporting an outer periphery of said semiconductor module].

3. The multilayer semiconductor device assembly jig according to claim 2, wherein said alignment mechanism comprises a plurality of positioning pins and positioning holes for receiving the positioning pins which are correspondingly formed [on an opening end of] in said box-shaped member and said mother substrate.

4. The multilayer semiconductor device assembly jig according to claim 1, wherein said position restriction mechanism further comprises a plurality of positioning pins [provided on] secured in said base member and which are used for [locking] securing at least three different [positions] portions of an outer periphery of said semiconductor [module] modules.

5. The multilayer semiconductor device assembly jig according to claim 1, wherein said position restriction mechanism further comprises a plurality of positioning pins provided [on said base member for piercing] secured in said base member and which pierce through positioning holes formed in [marginal regions of] said semiconductor modules.

6. The multilayer semiconductor device assembly jig according to claim 5, wherein said positioning [pin is]pins also [used for said alignment mechanism with a tip thereof piercing] pierce through a positioning hole formed on said mother substrate.

7. The multilayer semiconductor device assembly jig according to claim 1, wherein said height restriction mechanism [comprising] further comprises:

[a box-shaped member assembled on said base member and provided with a storage space therein for storing the specified number of said semiconductor modules in a layered state; and]

a cover member [assembled to said box-shaped member by pressing a top-layer semiconductor module placed in said storage space] secured over said semiconductor modules.

8. A multilayer semiconductor device manufacturing method using an assembly jig for mutually restricting positions of a plurality of semiconductor modules each including a semiconductor chip mounted on a thin printed wiring board [and a bump on each of a plurality of inter-layer connection lands through the use of a position restriction mechanism, layering said modules with an entire height restricted through the use of a height restriction mechanism, and maintaining evenness of a top-layer semiconductor module through the use of a evenness holding mechanism,] comprising the steps of:

serially layering the [specified number of said] semiconductor modules on [said] a base member with respective lateral positions restricted by [said] a lateral position restriction mechanism and placing [layered modules in] said assembly jig with an entire height of said layered modules restricted by said height restriction mechanism,

supplying said assembly jig into a reflow furnace, applying reflow heating to melt [said each bump] solder bumps and for thereby forming interlayer connection among said semiconductor modules, and thus forming a layered semiconductor module unit; and

mounting said layered semiconductor module unit on a mother substrate by using a top-layer semiconductor module as a junction module [with evenness maintained by said evenness holding mechanism].

9. The multilayer semiconductor device manufacturing method according to claim 8, further comprising a step of providing said assembly jig with an alignment mechanism for aligning said layered semiconductor module unit against said mother substrate [for mounting, comprising the steps of:

positioning and combining said assembly jig, inverted after forming layered semiconductor module unit, with said mother substrate via said alignment mechanism;

supplying an assembly of said assembly jig and said mother substrate into a reflow furnace and applying reflow heating for interlayer connection between a first layer semiconductor module in said layered semiconductor module unit and said mother substrate; and

removing said assembly jig from said mother substrate].

10. The multilayer semiconductor device manufacturing method according to claim 8 [using said printed-wiring board having interlayer connection lands and dummy lands corresponding to interlayer connection lands on all printed-wiring boards for respective layers,] further comprising the step of:

forming a bump on each of connection lands and dummy lands of [said] printed wiring board for each semiconductor module.

REMARKS

Applicants thank the Examiner for the indication of allowable subject matter in claims 8-10. By this amendment, applicants have modified claims 1-7 as well as 8-10 in order to more broadly define the presently claimed invention. Applicants submit that the newly modified claims are similarly allowable over the art of record.

Applicants submit that the modified claims have overcome the rejections set forth by the Examiner under 35 USC section 101, as well as the rejections set forth under 35 USC section 112, second paragraph.

In light of the foregoing Applicant respectfully requests that the Examiner issue a Notice of Allowance for this application.

Respectfully submitted,

Date: July 26, 2002

(Reg #37,607)

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1. A multilayer semiconductor device assembly jig, comprising:

a lateral position restriction mechanism for positioning a plurality of stacked semiconductor modules on a base member with their respective lateral positions mutually restricted;

a height restriction mechanism for restricting an entire height of said semiconductor modules layered on said base member; and

an alignment mechanism for providing alignment with reference to a mother substrate.

2. The multilayer semiconductor device assembly jig according to claim 1 comprising a box-shaped member which is positioned on said base member and having a storage space for storing said semiconductor modules in a layered state,

wherein an inner wall of said storage space constitutes said lateral position restriction mechanism.

3. The multilayer semiconductor device assembly jig according to claim 2, wherein said alignment mechanism comprises a plurality of positioning pins and positioning holes for receiving the positioning pins which are correspondingly formed in said box-shaped member and said mother substrate.

4. The multilayer semiconductor device assembly jig according to claim 1, wherein said position restriction mechanism further comprises a plurality of positioning pins secured in said base member and which are used for securing at least three different portions of an outer periphery of said semiconductor modules.

5. The multilayer semiconductor device assembly jig according to claim 1, wherein said position restriction mechanism further comprises a plurality of positioning pins provided secured in said base member and which pierce through positioning holes formed in said semiconductor modules.

6. The multilayer semiconductor device assembly jig according to claim 5, wherein said positioning pins also pierce through a positioning hole formed on said mother substrate.

7. The multilayer semiconductor device assembly jig according to claim 1, wherein said height restriction mechanism further comprises:

a cover member secured over said semiconductor modules.

8. A multilayer semiconductor device manufacturing method using an assembly jig for mutually restricting positions of a plurality of semiconductor modules each including a semiconductor chip mounted on a thin printed-wiring board comprising the steps of:

serially layering the semiconductor modules on a base member with respective lateral positions restricted by a lateral position restriction mechanism and placing said assembly jig with an entire height of said layered modules restricted by said height restriction mechanism,

supplying said assembly jig into a reflow furnace, applying reflow heating to melt solder bumps and for thereby forming interlayer connection among said semiconductor modules, and thus forming a layered semiconductor module unit; and

mounting said layered semiconductor module unit on a mother substrate by using a top-layer semiconductor module as a junction module.

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9. The multilayer semiconductor device manufacturing method according to claim 8, further comprising a step of providing said assembly jig with an alignment mechanism for aligning said layered semiconductor module unit against said mother substrate.

10. The multilayer semiconductor device manufacturing method according to claim 8 further comprising the step of:

forming a bump on each of connection lands and dummy lands of printed wiring board for each semiconductor module.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PRELIMINARY AMENDMENT ACCOMPANYING APPLICATION

APPLICANT: Yoshiyuki Yanagisawa, et al. ATTY. DOCKET NO. 09792909-5046

SERIAL NO.

DATE FILED:

INVENTION: "ASSEMBLY JIG AND MANUFACTURING METHOD OF MULTILAYER SEMICONDUCTOR DEVICE"

Assistant Commissioner of Patents
Washington, D.C. 20231

S I R:

Between the title and the heading "Background of the Invention" on page 1, insert the following:

A'

—RELATED APPLICATION DATA

The present application claims priority to Japanese Application No. P2000-171059 filed June 7, 2000, which application is incorporated herein by reference to the extent permitted by law.—

Respectfully submitted,

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